Chief Patron

Prof (Dr.) U.S. Sharma
Hon'ble Vice-Chancellor, MPUAT, Udaipur

Prof. Udaykumar R. Yaragatti
Director, MNIT, Jaipur

Patron

Dr. S.S. Rathore
Dean, CTAE, MPUAT, Udaipur

Organizing Chair

Dr. Sunil Joshi
Professor & Head, Department of ECE, CTAE, MPUAT

Prof. K.K. Sharma
Professor & Head, Department of ECE, MNIT

Coordinators

Dr. Navneet Agrawal, Asst. Professor ECE, CTAE
Dr. Chitrakant Sahu, Asst. Professor ECE, MNIT
Mr. Deep Manwar, Asst. Professor ECE, CTAE

Organizing committee

Dr. Mahesh Kothari, TEQIP Coordinator, CTAE
Dr. Rohit Bhakar, TEQIP Coordinator, MNIT
Dr. Deepak Sharma, Administrative Officer, CTAE
Dr. Naveen Choudhary, Computer science Engineering
Dr. R. R. Joshi, Electrical Engineering, CTAE
Dr. S. M. Mathur, Farm machinery and Engineering, CTAE
Dr. M. A. Saloda, Mechanical Engineering, CTAE
Dr. Anupam Bhatnagar, Mining Engineering, CTAE
Dr. P. S. Champawat, Processing and Food Engineering
Dr. Sudhir Jain, Renewable Energy Engineering, CTAE
Dr. H. K. Mittal, Soil and Water Engineering, CTAE
Dr. R. P. Arora, Civil Engineering, CTAE
Dr. A. K. Chittora, Basic Science, CTAE
Mr. Himanshu Mohan, Electronics and Communication
Ms. Prerna Dhull, Electronics and Communication
Mr. Vishwapriya, Electronics and Communication
Dr. Pranay Joshi, Electronics and Communication
Dr. Suriti Gupta, Electronics and Communication
Mr. Neeraj Chaoudhary, Electronics and Communication
Mr. Lalit Verma, Electronics and Communication
Ms. Durga Kumari, Electronics and Communication
Ms. Keerti Singhvi, Electronics and Communication
Mrs. Ankita Bapna, Electronics and Communication
Ms. Surbhi Mehta, Electronics and Communication
Ms. Rachna Mehta, Electronics and Communication

Joint Workshop
on

CMOS Digital IC Design: Concept and Recent Trends

(March 26-30, 2018)

REGISTRATION FORM

Name:**.....**

(In block letters)

Institution:**.....**

Address:**.....**

…….

Phone:**.....**

e-mail:**.....**

Details of Registration fee-

DD No. ..... Date: .....

Bank Name**.....**

Amount Rs**.....**

Date**.....** ***Signature of participant***

Contact us:

Mr. Deep Manwar
e-mail: *deep.manwar@gmail.com*
Phone: 07573042214

Student Coordinators
Shweta Jaroli
e-mail: *shweta.jaroli21@gmail.com*
Aditi Gaur
e-mail: *aditigaur075@gmail.com*

College of Technology and Engineering (CTAE) Udaipur

&

Malaviya Institute of Technology (MNIT) Jaipur

Jointly organizes

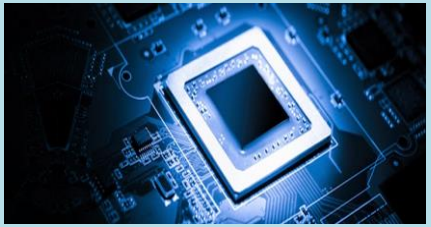
A Workshop on

CMOS Digital IC Design: Concept and Recent Trends

(March 26-30, 2018)

under

Technical Education Quality Improvement Programme



Venue
Department of Electronics and Communication Engineering, CTAE, MPUAT Udaipur-313001

ABOUT CTAE, UDAIPUR

The college of Technology and Engineering, Udaipur (CTAE) is a constituent college of the Maharana Paratap University of Agriculture and Technology (MPUAT), Udaipur. The college was started in 1964 with the graduate programme in Agricultural Engineering. Presently the CTAE has B.Tech programs in 8 branches, M.Tech programs in 12 disciplines and PhD. Programs in 9 disciplines. It is situated at about 7 km form Udaipur city railway station and bus terminal and 2 km from Rana Pratap Nagar railway station. The college is actively engaged in research and training in various disciplines of engineering. The college has undergone the MOUs and collaborations with a number of Indian and Foreign Organisation.

ABOUT DEPARTMENT OF ECE

The department of ECE has made significant contributions in research, training and teaching. The department has earned number of externally funded research projects sponsored by Department of Electronics and Information Technology, MCIT, Govt of India, AICTE, New Delhi, Department of Science and Technology, etc. and published significant research articles in the journal of high impact factor.

ABOUT TEQIP

CTAE has been bestowed with the prestigious Technical Education Quality Improvement Program (TEQIP) for strengthening institute to improve learning outcomes and employability of graduates by Ministry of Human Resource and Development, Government of India. This project is a World Bank initiative to improve efficiency and effectiveness of the technical education system.

OBJECTIVES OF THE WORKSHOP

The workshop mainly targets faculties and students working in the field of VLSI. This workshop will act as a platform for interaction with peers working in the same field. The workshop will provide an opportunity to understand the functioning, timing and power models of basic CMOS building blocks, various circuit topologies for implementing combinational, sequential logic and memories, transistor sizing and layout of different circuit topologies and also experience hands-on experiments. Learning EDA tools for schematic entry, layout, extraction and SPICE simulations will increase potential of candidates to find job and research opportunities in areas of VLSI, EDA design.

AREAS TO BE COVERED IN THE WORKSHOP

Introduction to semiconductor technologies, Introduction to CMOS Technology, CMOS Scaling challenges, CMOS Inverter Design, CMOS Layout Design rule, Static and Dynamic CMOS Logics, Memory Design, RC Delay mode, Fan out calculation and Ring Oscillator, Design, Logic Effort Calculation and methods, Testing of Memory Circuits., CMOS latch and flip-flop design and timing issues, sequential Design and Timing Analysis, Problem on sequential design and discussion, PLL Design, timing and power issues. Advance topics in CMOS such as FiNFET, Multigate Architecture and Advancement in Memory designs.

HANDS-ON SESSIONS

Simulation exercise on CMOS I-V characteristics, simulation exercise on CMOS Inverter Design, Simulation exercise on Static and Dynamic, CMOS Logic and Memory Design, exercise on Layout Design, Simulation exercise on Logical efforts, Simulation exercise on Logical efforts, Simulation sequential design, PLL design simulation, Feedback and Certificate Distribution.

SPEAKERS

Dr. Anand Bulusu, IIT Roorkee
Dr. Sunil Joshi, CTAE Udaipur
Dr. Amit M. Joshi, MNIT Jaipur
Dr. Chitrakant Sahu, MNIT Jaipur
Dr. Navneet Agarwal, CTAE Udaipur
Dr. Shubhankar Majumdar, NIT Meghalaya
Mr. Deep Manwar CTAE Udaipur

REGISTRATION

Students: Rs. 1,000/- , Faculty: Rs. 1500/-, Industry Rs. 2000 /-

The registration will be confirmed on 'First come first serve' basis. **Demand draft** in favour of "**DEAN Boys Fund, CTAE**" payable at Udaipur. The enclosed registration form along with Demand Draft should be posted to "**Organizing chair, Department of ECE, CTAE, MPUAT, Udaipur – 313001**".

The fee can also be paid through bank transfer at the given details
Name of the Bank: ICICI Bank
Branch: university campus, Udaipur
Name Account: Dean Boy's fund CTAE, Udaipur
A/C No & IFSC Code: 694201001275 & ICIC0006942

The enclosed registration form along with the scanned copy of transaction slip should be sent to the Organizing chair on suniljoshi7@rediffmail.com.
All the participants are supposed to fill the details on "https://goo.gl/forms/yHWHnR5vz6yT94Nw1"

IMPORTANT DATES

Last date for submission of application: **March 14, 2018**
Selection-list intimation/display before: **March 19, 2018**

GENERAL INFORMATION

Accommodation and travelling expenses are to be borne by the participants. Workshop kit and Lunch will be provided by the organizers. Brochure is available on institute web site www.ctae.ac.in

ELIGIBILTY AND NUMBER OF SEATS

The workshop can be attended by students of B. Tech, M. Tech, PhD and faculties of ECE Branch. 40 seats are available. 20 seats are reserved for faculties from TEQIP institutes.