Organized by
Electronics & ICT Academy

MNIT Jaipur
http://www.mnit.ac.in/eict

Mixed-Signal CMOS ICs
"Methodology of Circuit to Chip Design"

March 6 - 10, 2019
Venue: Academy, Prabha Bhawan, MNIT Jaipur
http://academymnit.wordpress.com

Faculty Development Programme
Sponsored by

Department of Electronics & Information Technology
Ministry of Communications & Information Technology
Government of India

Ministry of Electronics & Information Technology
Government of India
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Chairman, Advisory Board, EICT Academy & Director MNIT Jaipur
Prof. Udaykumar R. Yaragatti

Honorary Academic Chair, EICT Academy
Prof. V. Sinha

Chief Investigator, EICT Academy
Prof. Vineet Sahula, ECE

Co- Chief Investigators, EICT Academy
Dr. L. Bhargava, ECE
Dr. Pilli Emmanuel Shubhakar, CSE
Dr. C. Periasamy, ECE
Dr. S. J. Nanda, ECE
Head, ECE (Prof. D. Boolchandani)
Head, CSE (Prof. Girdhari Singh)

Preamble (Electronics & ICT Academy)
Government of India had announced a National Policy on Skill Development, which has set a target of skilling 500 million people by 2022 in the domain of Electronics & IT. Under the plan scheme of "Digital India Manpower Development". MeitY has set up seven (07) Electronics and ICT Academies as a unit in 03 IITs, 03 NITs and 01 IIIT with an objective of faculty/mentor development/up gradation in the areas related to Electronics & ICT leading ultimately to improved employability of graduates/diploma holders. MNIT Jaipur has set up such an academy for providing specialized training to faculty and industry persons in the states/UTs of Rajasthan, Gujarat, Daman & Diu, Dadra Nagar Haveli.

(A) Issues-
1. IT Hardware and Electronics Manufacturing industry- availability of properly trained, skilled and qualified manpower
2. Number of quality PhDs generated in IT / Computer Science is very low
3. In E & ICT domain- there is a very high degree of obsolescence of existing technologies and faster emergence of newer technologies

(B) Approach-
1. A focused faculty training/updation programme for IT, Electronics and related sectors
2. Spreading up and continuous updation regarding Emerging Technology
3. Training and consultancy services for Industry
4. Design, Develop and Deliver specialized modules for specific research areas and Industry
5. Providing advice and support for technical incubation and entrepreneurial activities

An intensive one-week training programme is being organized for faculty of engineering and technological institutions. It is also open to persons from industry and doctoral students of Indian organizations. The objective is to provide an exposure to the participants to the state-of-the-art in Design and analysis of mixed-signal circuit & sub-systems. The participants will be given exposure to circuit to chip design process through EDA Tools. Experts are from SCL Chandigarh including host institution. The technical program will include state-of-the-art lectures, hands-on lab sessions, tool demonstrations, and discussion/presentation sessions.

Programme Topics:
Challenges in Deep sub-Micron CMOS Technology for mixed signal design, Current Mirrors, switch capacitors, differential amplifiers and two stage OPAMPs design. Comparators, Regenerative time constant, Comparator Non-idealities. Flash ADC, Pipeline ADC and DAC, Performance analysis Metrics of ADCs and DACs. EDA Tools methodology on mixed-signal circuit to chip design.

Invited Experts:
Senior Scientist from SCL Chandigarh having more than 10 years of experience in CMOS device/circuit fabrication and chip design.

Programme Coordinators:

Prof. D. Boolchandani	dboolchandani.ece@mnit.ac.in	9549654229 (M)
Dr. Tarun Varma	tvarma.ece@mnit.ac.in	9549654230 (M)
Dr. Chitrakant Sahu	chitrakant.ece@mnit.ac.in	9549655371 (M)

Registration:
Registration is open to faculty, industry persons, doctoral and postgraduate students of programmmes related to Electronics and Communication/Electrical & Electronics / Computer Science Enginerring.
Participants will be admitted on first-come first-served basis.
Register on line at - http://www.mnit.ac.in/eict/acad_training_prg.php

Fee:
(A) The one-time registration fee of Rs. 500/- is to be paid by each participant attending first time, irrespective of affiliation. This fee is not applicable for those participants, who have attended any academy training programme earlier.
(B) (i) The participants from academia and research scholars are required to pay a further fee of Rs. 2000/- (faculty/research-scholars). Rest expenditure is sponsored by MeitY through Electronics & ICT Academy at MNIT Jaipur.
(ii) The participants from industries, UG/PG students are required to pay a further fee of Rs. 5000/-.
(iii) Applicable relaxation for SC/ST candidate is 50%.
(iv) Fee once paid will not be refunded back, however, it may be adjusted to another FDP.
(C) The fee covers the participation in the programme, registration material including tutorial notes, boarding (breakfast/lunch) on all the days of the workshop. The travel and other expenses would have to be borne by the participants or their parent-organizations.
(D) Complimentary lodging for a very limited number of participants is available in Guest rooms of Aurobindo hostel. Also, accommodation in Guest-house-2 can be arranged on first-come first-serve and additional payment basis.
(E) The organizers should receive the registration amount through online payment/NEFT/IMPS.

Account Name- 'Electronics and ICT Academy MNIT Jaipur'	Account Number- 676801700483
Bank address- ICICI Bank, MNIT Campus Branch, Jaipur	IFSC Code- ICIC0006768

(F). Please pre-intimate your desire to participate and for accommodation to programme coordinator through e-mail, immediately after online registration.
→For any other query else then this FDP, **email us at** academy@mnit.ac.in