

Dept. of ECE, MNIT Jaipur

Time Table

I Semester M. Tech. VLSI

Odd Semester 2021-22

	8-9 AM	9-10 AM	10-11 AM	11-12 PM	12-1 PM	1-2 PM	2-3 PM	3-4 PM	4-5 PM	5-6 PM
Monday		21ECT543 Dig. IC Design C.P VLTC-L104	21ECT839 CAD VLSI LB VLTC-L104		21ECT542 Ana. IC Design DB VLTC-L104	Lunch				
Tuesday		21ECT541 Adv. Sem. Dev. C.S VLTC-L104	21ECT544 Reduced Order Mod., opt. and Int. VS VLTC-L104	21ECT542 Ana. IC Design DB LT-L104	21ECT842 Dig. Sys. Des. D.Bharti VLTC-L104					
							PG-V Sem. Device and IC Lab – 1; VLSI Lab; VS,DB			
Wednesday		21ECT541 Adv. Sem. Dev. C.S VLTC-L104	21ECT544 Reduced Order Mod., opt. and Int. VS VLTC-L104		21ECT833 VLSI Sig. Proc AMJ VLTC-L104		21ECT842 Dig. Sys. Des. D.Bharti VLTC-L104			
Thursday		21ECT543 Dig. IC Design C.P VLTC-L104	21ECT839 CAD VLSI LB VLTC-L104	21ECT833 VLSI Sig. Proc AMJ VLTC-L104	21ECT542 Ana. IC Design DB VLTC-L104					
							PG-V Sem. Device and IC Lab – 1; VLSI Lab; VS,DB			
Friday		21ECT543 Dig. IC Design C.P VLTC-L104	21ECT839 CAD VLSI LB VLTC-L104	21ECT842 Dig. Sys. Des. D.Bharti VLTC-L104	21ECT833 VLSI Sig. Proc AMJ VLTC-L104		21ECT541 Adv. Sem. Dev. C.S VLTC-L104			

(Dr. Bharat Choudhary)

(Dr. Rajesh Saha)

(Prof. Vijay Janyani)