# Master of Technology in VLSI Design
## Department of Electronics & Communication Engineering

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Course Title</th>
<th>Credit</th>
<th>Total (L T P)</th>
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<tbody>
<tr>
<td><strong>Semester 1 (Core Courses)</strong></td>
<td></td>
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<tr>
<td>ECT601</td>
<td>Digital CMOS ICs</td>
<td>3</td>
<td>(3-0-0)</td>
</tr>
<tr>
<td>ECT603</td>
<td>CAD Algorithms for Synthesis of Digital Systems</td>
<td>3</td>
<td>(3-0-0)</td>
</tr>
<tr>
<td>ECT605</td>
<td>Digital System Design</td>
<td>3</td>
<td>(3-0-0)</td>
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<tr>
<td>ECT607</td>
<td>CAD Algorithms for VLSI Physical Design</td>
<td>3</td>
<td>(3-0-0)</td>
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<tr>
<td>ECP611</td>
<td>System Design lab-1</td>
<td>3</td>
<td>(0-0-6)</td>
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<tr>
<td>ECT631</td>
<td>Analog &amp; Mixed Signal ICs</td>
<td>3</td>
<td>(3-0-0)</td>
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<tr>
<td>ECT990</td>
<td>Mathematical Methods &amp; Techniques for ECE technologists-I</td>
<td>3</td>
<td>(3-0-0)</td>
</tr>
<tr>
<td>ECT992</td>
<td>Mathematical Methods &amp; Techniques for ECE technologists-II*</td>
<td>3</td>
<td>(3-0-0)</td>
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<tr>
<td><strong>Total Semester Credits</strong></td>
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| **Semester 2 (2 + 5 electives)** | | | |
| ECP612 | System Design lab-2 | 3 | (0-0-6) |
| ECD656 | Minor Project | 4 | (0-0-8) |
| (Elective Courses)# | | | |
| ECT614 | VLSI Technology | 3 | (3-0-0) |
| ECT616 | Computer Arithmetic & Micro-architecture Design | 3 | (3-0-0) |
| ECT618 | Graph Algorithms & Combinatorial optimization | 3 | (3-0-0) |
| ECT620 | Microelectronic Devices & Circuits | 3 | (3-0-0) |
| ECT622 | System Level Design & Modeling | 3 | (3-0-0) |
| ECT624 | VLSI Testing & Testability | 3 | (3-0-0) |
| ECT626 | Formal Verification of Digital Hardware & Embedded Software | 3 | (3-0-0) |
| ECT628 | Memory design & testing | 3 | (3-0-0) |
| ECT630 | Advanced Computer Architecture | 3 | (3-0-0) |
| ECT632 | Embedded systems Design | 3 | (3-0-0) |
| ECT634 | Micro- & Nano- electro-mechanical Systems (MEMS & NEMS) | 3 | (3-0-0) |
| ECT638 | Design of Asynchronous Sequential Circuits | 3 | (3-0-0) |
| ECT640 | Electronic manufacturing Technology | 3 | (3-0-0) |
| ECT642 | FPGAs Physical Design | 3 | (3-0-0) |
| ECT650 | Special Topics in VLSI-1 | 3 | (2-0-2) |
| ECT652 | Special Topics in VLSI-2 | 3 | (2-0-2) |
| ECT654 | RF Integrated Circuits | 3 | (3-0-0) |
| ECT656 | Adaptive Signal Processing | 3 | (3-0-0) |
| ECT657 | VLSI signal processing architectures | 3 | (3-0-0) |
| ECT658 | Current-Mode Analog Signal processing | 3 | (3-0-0) |
| **Total Semester Credits** | | | 22 |

| **Semester 3** | | | |
| ECD659 | Dissertation | 16 | (0 0 32) |
| **Total Semester Credits** | | | 16 |

| **Semester 4** | | | |
| ECD660 | Dissertation | 16 | (0 0 32) |
| **Total Semester Credits** | | | 16 |

**Total Credits of all semesters**: 75

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# These courses will be offered by the faculty of Department.
# The students may opt for any of the elective course offered in the Institute on recommendation of supervisor
* only one course out of ECT990 or ECT992 shall be offered and ONLY one is required to be opted.
# PG Course Details

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<tbody>
<tr>
<td>Course Code: ECT-601</td>
<td>Course Name: Digital CMOS ICs</td>
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<tr>
<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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</table>

**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**

Process flow and masking steps for MOS and CMOS technologies, Lambda based design rules- Electrical behavior of MOS transistors; Latch up in CMOS technology.

Layer properties of various conducting layers in MOS technology (diffusion, poly-silicon and metal): Sheet resistance, relative capacitance.

Fundamental time constant ($\tau$) for a technology.

Design and analysis of NMOS (enhancement and depletion) and CMOS inverters; rationing of transistor size, logic threshold, logic low voltage level, rise and fall of delays.

Design of basic gates in NMOS technology; CMOS logic design styles: static CMOS logic (AND, NOR gates), complex gates, domino logic, pseudo NMOS logic, clocked CMOS (C2 MOS) logic.

Structured logic design: programmable arrays.

Design of latches and flip-flops, static memory cell and dynamic memory cell. Sense amplifier- necessity, design, and influence of Sense Amplifier on cell Architecture.

MOS scaling theory and scaling of interconnection.

**Books:**


Course Code: ECT990  Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-I

Credit: 3  L-T-P: 2-1-0

Pre-requisite course:

Co-requisite course:

Syllabus:

[The following contents have implicit application to and exemplification through ECE problems such as communication over unreliable channel, processing of random signals, amplitude modulation by random signals, reliability of an electronic/communication systems, resource sharing in a system, and networks of queues]

A. Applied Probability and probability models: one- and two-dimensional random variables (RVs); discrete RVs- Poisson, geometric, binomial, hyper-geometric & multi-model; continuous RVs- normal, exponential, Gamma, chi-square, bivariate normal; moment generating function & Laplace of RV distribution; Random processes; Markov chain- continuous, discrete; Poisson process; renewal theory; queuing theory; reliability theory; 16 Hrs.

B. Brownian motion & stationery processes; Computer methods for generating RVs; Simulation- general & special techniques for continuous and discrete distributions, multi-variate distributions; variance reduction techniques; Monte-Carlo techniques 05 Hrs.

C. Transforms & systems analysis- Fourier Series, Fourier transform, z-transform, discrete cosine (sine) transform, Wavelet transform, fractional transforms. 07 Hrs.

Suggested references (not limited to)-

Further references
1. Discrete Wavelet transforms, Patrick J. Van Fleet, Wiley Interscience, 2007
**Program:** M. Tech. (VLSI Design)  
**Department:** Electronics & Comm. Engg.  

<table>
<thead>
<tr>
<th>Course Code: ECT 992</th>
<th>Course Name: Mathematical Methods and techniques for Electronics &amp; Communication Technologists-II</th>
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<tbody>
<tr>
<td>Credit: 3</td>
<td>L-T-P: 2-1-0</td>
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</table>

**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**

*The following contents implicit application to and exemplification through ECE problems such as reduced order polynomials, order reduction of a transfer function, sparse matrix based solution of large systems, implementation of search algorithms for design space exploration]*

A. Linear algebra and Matrix analysis – Groups, fields and rings; vector spaces; basis & dimensions; canonical forms; inner product spaces- orthogonalization, Gram-Schmidt orthogonalization, unitary operators, change of orthonormal basis, diagonalization; eigenvalues & eigen vectors- Gerschgorin theorem, iterative method, Sturm sequence, QR method, introduction to large eigen value problems. 10 Hrs.

B. Function approximation & reduced order modelling of systems- Taylor's polynomial, least square approximation, Chebyshev series/polynomial, splines, Pade & rational approximation, Krylov subspaces, Lanczos process, Arnoldi method; Symbolic analysis and reduced order modelling of interconnects, linear and weakly non-linear analog/digital systems 12 Hrs.

C. Combinatorial optimization- counting methods, algorithms for optimization 06 Hrs.

**Suggested references** (not limited to)-

4. Combinatorial optimization, Papadimitriou and Steiglitz, PHI (I)

**Further references**

2. Y. Saad, Numerical methods for large Eigenvalue problems, [www.umn.edu](http://www.umn.edu)
3. Matrix Analysis & linear algebra, Meyer, SIAM
4. Schaum’s outline on Linear Algebra, McGraw Hill
5. H. A. van der Vorst, Iterative methods for large linear systems, citeseerx.ist.psu.edu
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<tr>
<td>Course Code: ECT-603</td>
<td>Course Name: CAD Algorithms for Synthesis of Digital Systems</td>
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<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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</table>

**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**

Role of CAD in digital system design, levels of design, modeling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping;

CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as microprogrammes, PLAs, gate arrays etc. Technology mapping for FPGAs.

Low power issues in high level synthesis and logic synthesis.

**Books:**

4. N. Deo, Graph Theory, PH India.
### Program: M. Tech. (VLSI Design)  

<table>
<thead>
<tr>
<th>Course Code: ECT-605</th>
<th>Course Name: Digital System Design</th>
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<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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### Pre-requisite course:

### Co-requisite course:

### Syllabus:
- Sequential Logic Design- Introduction, Basic Bistable Memory Devices, additional bistable devices, reduced characteristics and excitation table for bistable devices.
- Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Mealy Machines,
- Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs.
- Data path and Control design.
- Introduction to VHDL/Verilog- Data types, Concurrent statements, sequential statements, behavioral modeling.
- Introduction to programmable logic devices- PALs, PLDs, CPLDs and FPGAs.

### Books:
### Syllabus:

**Problem-set for algorithm implementation:**

Boolean algebraic formulations

- a. Covering algorithm - Brach & bound
- b. ROBDD computation
- c. Operation between ROBDDs: ‘+’, ‘.’

**Graph based optimization**

- a. Two consideration each
- b. Two consideration each
- c. Graph coloring
- d. Clique partitioning
- e. Edge covering
- f. Vertex covering
- g. Independent set finding

**List scheduling**

- a. Latency constrained resource minimization
- b. Resource constrained latency minimization
- c. Path based scheduling
- d. Pipelined data-path scheduling
- e. Hu’s multiprocessor scheduling

**Allocation & binding**

- a. FU binding
  - a. Coloring
  - b. Clique finding
  - c. Left edge based binding
- b. Storage unit binding
  - a. Coloring
  - b. Clique finding
  - c. Left edge based binding
- c. Interconnect binding
  - a. Coloring
  - b. Clique finding
  - c. edge based binding

### Books:
Program electives-

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<tr>
<td>Course Code: ECT-616</td>
<td>Course Name: Computer Arithmetic &amp; Micro-architecture Design</td>
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<tr>
<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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Pre-requisite course:

Co-requisite course:

Syllabus:

Computer arithmetic- conventional & higher radix number systems, residue & logarithmic number systems; sequential & parallel (and high speed) algorithms for addition, multiplication, division; evaluation of elementary functions- sin, cos, sin⁻¹, cos⁻¹, sinh etc; CORDIC method for trigonometric functions; languages for design description (HDLs) like VHDL or Verilog; Modeling and simulation of circuits at various levels;

Data path design for high performance- pipelining & systolic arrays; Control design- sequential, hardwired & micro-programmed control.

Topics in design-yield and redundancy,

Low power design techniques.

Books:

For Review


Computer arithmetic

2. Ercegovac, Digital Systems, Wiely, 2004

For Data-path/Control Design


For HDLs

9. Palnitkar, Verilog…., Pearson India/Prentice-Hall India

Low power design

11. Mead & Conway. VLSI circuit design
14. K. Roy and et al, Low power design, Wiley
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<tr>
<td>Course Code: EV-501</td>
<td>Course Name: Digital CMOS ICs</td>
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<tr>
<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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Pre-requisite course:

Co-requisite course:

**Syllabus:**
- Graph Theory- basics, Planarization, triangulation, graph algorithms for shortest/longest paths, spanning tree, search etc.
- Optimization problem- Convex sets and functions.
- The SIMPLEX algorithm- forms of linear programming problem, geometry of LP, organization of Tableau. Computational considerations for simplex algorithm
- Algorithms & complexity- shortest path, max-flow, Dijkstra’s algorithm, min-cost flow, algorithm for graph search and matching; spanning trees and matroids; Integer Linear programming, Greedy algorithm, approximation algorithms; branch-and-bound; dynamic programming.

**Books:**
1. Narsingh Deo, Graph theory, Prentice Hall India, 2008.
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<tr>
<td>Course Code:</td>
<td>ECT-624</td>
<td>Course Name:</td>
<td>VLSI Testing &amp; Testability</td>
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<tr>
<td>Credit:</td>
<td>3</td>
<td>L-T-P:</td>
<td>3-0-0</td>
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**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**
- Physical Faults and their modeling; Stuck at Faults, Bridging Faults; Fault collapsing; Fault Simulation: Deductive, Parallel, and Concurrent Fault Simulation. Critical Path Tracing;
- ATPG for Combinational Circuits: D-Algorithm, Boolean Differences, PODEM Random, Deterministic and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.
- PLA Testing, Cross Point Fault Model and Test Generation.
- Memory Testing- Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests; Delay Faults.
- ATPG for Sequential Circuits: Time Frame Expansion; Controllability and Observability Scan Design, BILBO, Boundary Scan for Board Level Testing; BIST and Totally self checking circuits.
- System Level Diagnosis & repair- Introduction; Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes.
- Reconfiguration Techniques; Yield Modeling, Reliability and effective area utilization.

**Books:**
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<tr>
<td>Course Code: EV-614</td>
<td>Course Name: VLSI Technology</td>
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<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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</table>

**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**
- Basic IC processing steps.
- Crystal growth and wafer preparation.
- Epitaxy – basics of vacuum deposition, MBE. CVD - low and high temp/pressure depositions.
- Oxidation – properties of oxides, theory of oxidation, oxidation under different ambients.
- Ion implantation.
- Etching techniques.
- CVD of polysilicon, oxides and nitrides.
- Integrated circuit structures in bipolar and MOS.
- Introduction to process simulation, SUPREM.

**Books:**
**PG Course Details**

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<tr>
<td>Course Code: EC-620</td>
<td>Course Name: Microelectronic Devices &amp; Circuits</td>
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<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**

Brief recapitulation- band theory, FD statistics, recombination effects and bipolar junction devices. MOS devices-MOS capacitance, interface effects and characterization. MOSFET principles and characteristics, subthreshold region.

Various MOS structures-VMOS, DMOS etc. Parasitic effects in MOSFET and bipolar circuits. CCDs. High frequency devices-metal semiconductor contacts. MESFETS.

Hetero-junction devices-HEMTs, HBTs.

Device modeling: Bipolar devices-Gummel –Poon model and RC Distributed model.

MOS device modeling-long channel effects short channel structures scaled down device models, subthreshold conduction.

**Books:**

# PG Course Details

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<td>Course Code: EV-650</td>
<td>Course Name: Special Topics in VLSI Design-1</td>
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<td>Credit:3</td>
<td>L-T-P: 2-0-2</td>
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## Pre-requisite course:

## Co-requisite course:

## Syllabus:
System modeling aspects for digital & analog systems; reduced order modeling for linear and non-linear systems; analog macromodeling & synthesis.

## Books:
Relevant conference/journal papers.
### PG Course Details

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<tr>
<td><strong>Course Code:</strong> EV-607</td>
<td><strong>Course Name:</strong> CAD Algorithms for VLSI Physical Design</td>
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<tr>
<td><strong>Credit:</strong> 3</td>
<td><strong>L-T-P:</strong> 3-0-0</td>
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**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**

- FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis.

**Books:**

## PG Course Details

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<td>Course Code:</td>
<td>EV-622</td>
<td>Course Name:</td>
<td>System Level Design &amp; Modeling</td>
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<td>Credit:</td>
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<td>L-T-P:</td>
<td>3-0-0</td>
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### Pre-requisite course:

### Co-requisite course:

### Syllabus:
- System level design, description languages- SystemC, SDL, SpecChart etc.
- Architectural synthesis for DSP applications.
- Formal Verification of digital hardware systems- BDD based approaches, functional equivalence, finite state automata, automata, FSM verification. Model checking.

### Books:

1. Gajski, Gupta and Vahid, Specifications and design of Embedded systems
2. Topics on formal verification to be covered using topics from literature.
## PG Course Details

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<td>Course Code: ECT-631</td>
<td>Course Name: Analog and Mixed Signal ICs</td>
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<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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### Pre-requisite course:

### Co-requisite course:

### Syllabus:
- Theory and design of MOS Operational Amplifier, Complete CMOS operational amplifier including frequency compensation. Comparators and Voltage Reference Sources.
- Switched Capacitor Circuits: Principles of operation of Switched Capacitor Circuits, Switched Capacitor Filters.
- D/A and A/D converters.
- Nonlinear Analog circuits: Timers, Function generators, Multipliers and PLL.

### Books:
## PG Course Details

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<tr>
<td>Course Code: ECT-626</td>
<td>Course Name: Formal Verification of Digital Hardware &amp; Embedded Software</td>
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<tr>
<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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### Syllabus:
- Formal Verification of digital hardware systems- BDD based approaches, functional equivalence, finite state automata, -automata, FSM verification. Model checking; various industry & academia CAD tools for formal verification.
- Verification, validation & testing - Debugging techniques for embedded software, instruction set simulators, clear box technique, black box testing, evaluating function test.

### Books:
2. J. W. Valvano, Embedded microcomputer systems- Real Time Interfacing, Thomson press (Cengage India)
7. Readings in Hardware/Software codesign, Micheli, Ernst, Wolf, Morgan Kaufmann.
## PG Course Details

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<td>Course Code: <strong>ECT628</strong></td>
<td>Course Name: <strong>Memory Design &amp; Testing</strong></td>
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<td>Credit: 3</td>
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### Pre-requisite course:

### Co-requisite course:

### Syllabus:

- Processing technology for Memories: Multipoly Floating Gate and Control Gate, Trench Capacitors and thin Oxide.
- Memory Modeling and testing faults in SRAMs, Marching Tests; Delay Faults.
- Semiconductor memory architecture, Space of memory faults- fault primitives.
- Preparation of Circuit Simulation: Definition & location of open, short, and bridge fault, Simulation methodology.
- Test for single cell and two port SRAMs, Functional fault modeling and testing of RAMs,
- Fault Diagnosis & Repair Algorithms.
- Built –in self Test and design for testability of RAMs.
- Built in self repair architecture.
- Trend in Embedded Memory testing.

### Books:

PG Course Details

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<td>Course Code: ECP612</td>
<td>Course Name: System Design Lab - 2</td>
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<td>Credit: 3</td>
<td>L-T-P: 0-0-6</td>
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Pre-requisite course:

Co-requisite course:

Syllabus:

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<tr>
<th>S. No</th>
<th>Objective Of Experiment</th>
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<tbody>
<tr>
<td>A-1</td>
<td>Design- (i) Full adder, D-FF; &amp; (ii) synthesis of combinational &amp; Sequential Components- 4-bit adder, 4-bit shift register, sequence detector (“1010”)</td>
</tr>
<tr>
<td>A-2</td>
<td>Layout synthesis of already designed (1st Odd Semester) Data Path &amp; Control for an arithmetic/logic application. Synthesis Using SYNOPSYS/CADENCE tool</td>
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Individual Application/Problems:
1. GCD-computer (4-bit)
2. Booth multiplier (4-bit)
3. 4-pt FFT
4. 4-pt IFFT
5. CORDIC for SinΘ/CosΘ
6. CORDIC for Sin^-1Θ/Cos^-1Θ
7. Non-Linear function exp(-2.5)/Sin 1.45/ Cos3.1/Sinh2.5/ Cosh3.2/log-natural
8. Find Average of Floating Point Numbers in Array of Size 16/32/64/128

1. For pseudo exhaustive TPG set T for BIST, follow the theorem concerning logical segmentation, which relates n (inputs), k (subspaces of size k among n), w (weight of n-tuple). Indicate w as well as |T_c| for different c; and n=20, k=3. Take example circuits/sub-systems for implementing the scheme & generating/applying random test patterns.
2. A circuit implementing f=xy+yz is to be tested using the syndrome-test method. Show that the faults z s-a-0 and z s-a-1 are not detected, while all other single stuck-at faults are detected. Arrange for experimental setup for all such testable as well as non-testable faults.
3. In a shift register polynomial division method of compression, a type 2 LFSR with P*(x)=1+x^2+x^4+x^5 is to be used for input sequence 1 1 1 1 0 1 0 1 (8 bits). Compute signature for the input sequence. Indicate at least one more input sequence, which would alias the given sequence. Arrange for experimental setup for verifying your design.

Books:

DPGC Convener                      Head, ECE          SPGB Chairman
# PG Course Details

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<tr>
<td>Course Code: ECT630</td>
<td>Course Name: Advanced Computer Architecture</td>
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<td>L-T-P: 3-0-0</td>
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## Pre-requisite course:

## Co-requisite course:

### Syllabus
- System Buses.
- Memory systems and error detection and error correction coding.
- Input/Output Modules & organization.
- Operating System Support.
- Instruction formats, instruction sets and their design, Pipelining.
- CPU Structure & RISC Architectures.

### Books:
## PG Course Details

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<td>Course Name: Embedded Systems</td>
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<td>Credit: 3</td>
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</tbody>
</table>

### Pre-requisite course:

### Co-requisite course:

### Syllabus

- Embedded computing- Microprocessors, embedded design process, system description formalisms. Instruction sets- CISC and RISC;
- CPU fundamentals- programming I/Os, co-processors, supervisor mode, exceptions, memory management units and address translation, pipelining, super scalar execution, caching, CPU power consumption.
- Embedded computing platform- CPU bus, memory devices, I/O devices, interfacing, designing with microprocessors, debugging techniques.
- Program design and analysis- models of program, assembly and linking, compilation techniques, analysis and optimization of execution time, energy, power and size.
- Processes and operating systems- multiple tasks and multiple processes, context switching, scheduling policies, inter-process communication mechanisms.
- Hardware accelerators- CPUs and accelerators, accelerator system design.
- Networks- distributed embedded architectures, networks for embedded systems, network-based design, Internet-enabled systems.
- System design techniques- design methodologies, requirements analysis, system analysis and architecture design, quality assurance.

### Books:

# PG Course Details

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<tbody>
<tr>
<td>Course Code: ECT634</td>
<td>Course Name: Micro&amp; Nano Electro Mechanical System (MEMS &amp; NEMS)</td>
</tr>
<tr>
<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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**Pre-requisite course:**

**Co-requisite course:**

## Syllabus
- Micro Electro Mechanical System (MEMS) Origins. MEMS Impetus / Motivation.
- Microwave MEMS Applications: MEM Switch Design Considerations. The Micromachine Transmission Line. MEMS-Based Microwave Circuit and System.

## Books:
# PG Course Details

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<tbody>
<tr>
<td>Course Code: ECT638</td>
<td>Course Name: Design of Asynchronous Sequential Circuits</td>
</tr>
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<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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</table>

### Pre-requisite course:

### Co-requisite course:

### Syllabus


Circuit Classification: Bounded Delay, speed independent, and delay independent. Data models (single-rail, dual-rail).

Handshaking protocols (2 phase, 4 phase)

Micropipeline Circuits: Basic building blocks. Pipelines, with and without data processing elements. The design of the Amulet processors.

NCL Logic: The NULL convention logic approach. Preserving delay insensitivity, threshold gates with hysteresis.

Formal Aspects of Asynchronous: The Rainbow approach. Green descriptions of micro-pipelines. Overview of formal basis to asynchronous descriptions

### Books:

1. Asynchronous sequential circuits by Stephen H. Unger, John Wiley & Sons
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<tbody>
<tr>
<td>Course Code: ECT640</td>
<td>Course Name: Electronic manufacturing Technology</td>
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<td>Credit: 3</td>
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**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**

**Books:**
## PG Course Details

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<tr>
<td>Course Code: ECT642</td>
<td>Course Name: FPGAs Physical Design</td>
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<td>Credit: 3</td>
<td>L-T-P: 2-0-2</td>
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</table>

### Pre-requisite course:

### Co-requisite course:

### Syllabus:
- Introduction to FPGA Architectures.
- FPGA design flow, partitioning, placement and routing algorithms.
- Technology mapping for FPGAs, case studies.

### Books:
## PG Course Details

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<tbody>
<tr>
<td>Course Code: ECT652</td>
<td>Course Name: Special Topics in VLSI Design-2</td>
</tr>
<tr>
<td>Credit:3</td>
<td>L-T-P: 2-0-2</td>
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</table>

### Pre-requisite course:

### Co-requisite course:

### Syllabus

Low power and low energy synthesis for digital systems, power estimation and modeling, power issues at system, algorithm, architecture and OS level, power issues in memory. Low power applications.

### Books:

Relevant conference/journal papers.
<table>
<thead>
<tr>
<th><strong>Program:</strong> M. Tech. (VLSI Design)</th>
<th><strong>Department:</strong> Electronics &amp; Comm. Engg.</th>
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<tr>
<td><strong>Course Code:</strong> ECT 658</td>
<td><strong>Course Name:</strong> Current-Mode Analog Signal Processing</td>
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<tr>
<td><strong>Credit:</strong> 3</td>
<td><strong>L-T-P:</strong> 3-0-0</td>
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</table>

**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**


**Suggested references (not limited to):**

5. Latest research papers on the topics mentioned in the syllabus.
### Program: M. Tech. (VLSI Design)

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<tbody>
<tr>
<td><strong>Course Code:</strong> ECT 657</td>
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<tr>
<td><strong>UG Code:</strong> ECT 468</td>
</tr>
<tr>
<td><strong>Course Name:</strong> VLSI based Signal Processing Architectures</td>
</tr>
<tr>
<td><strong>Credit:</strong> 3</td>
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<td><strong>L-T-P:</strong> 3-0-0</td>
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### Pre-requisite course:

### Co-requisite course:

### Syllabus:

**Introduction for DSP algorithms**: VLSI Design flow, Mapping algorithms into Architectures: Graphical representation of DSP algorithms – signal flow graph (SFG), data flow graph (DFG), critical path, dependence graph (DG). Data path synthesis, control structures, Optimization at Logic Level and architectural Design, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of Multirate data-flow graphs.

**Parallel and pipeline of signal processing application**: Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures; Pipelining processing of Digital filter, Parallel processing, Parallel and pipelining for Low power design, Optimization with regard to speed, area and power, asynchronous and low power system design, ASIC (application specific integrated circuits) and ASISP application specific instruction set processors) design;

**Systolic Array Architecture**: Methodology of systolic array architecture, FIR based Systolic Array, Selection of Scheduling Vector, Matrix multiplication of systolic array

**Architecture of different signal processing modules**: Convolution technique, Retiming concept, Folding /Unfolding Transformation, CORDIC architecture

**Low power Design**: Theoretical background, Scaling v/s power consumption, power analysis, Power reduction techniques, Power estimation approach

**Application in communication and signal processing system**: Transformation architectures, source and channel coding structures, Motion Estimation and motion compensation for video, Speech processing algorithm

### Suggested references (not limited to)-

3) M.A. Bayoumi, VLSI Design Methodology for DSP Architectures, Kluwer, 1994
4) U. Meyer – Baese, Digital Signal Processing with FPGAs, Springer, 2004
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<tr>
<td>Course Code: ECT 656</td>
<td>Course Name: Adaptive Signal Processing</td>
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<td>UG Code : ECT 467</td>
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<td>Credit: 3</td>
<td>L-T-P: 3-0-0</td>
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**Pre-requisite course:**

**Co-requisite course:**

**Syllabus:**

**Adaptive Filter Structures and Algorithms:**
Introduction to Adaptive systems, Adaptive Linear combiner, Minimum Mean-Square Error, Wiener-Hopf Equation, Error Performance Surface, LMS algorithm, Convergence of weight vector, Learning Curve, FX-LMS algorithm (Filtered X-LMS) and its application to ANC, Types of LMS, RLS algorithm, Matrix Inverse Lemma for RLS, Computational complexity of LMS and RLS, Convergence Analysis.

**Advancements in Transforms:**
Short time Fourier Transform (STFT), Multi Resolution Analysis, Wavelet Transform, Continuous Wavelet Transform (CWT), Inverse CWT, Discrete Wavelet Transform, Sub-band coding and implementation of DWT, Applications (signal and image compression, de-noising, detection of discontinuous and breakdown points in signals), S-transform, Frequency selective filtering with wavelet and S-transform.

**Applications:**
Direct Modelling or System Identification, Inverse Adaptive Modelling (Equalization), Adaptive Noise Cancellation, Adaptive filters for time series and stock market prediction, Biomedical Applications (Cancellation of 50-Hz interference in Electro-Cardiography, Cancelling donor heart interference in heart-transplant electrocardiography, Cancelling Maternal ECG in Fetal Electrocardiography), Echo Cancellation in Long distance Telephone Circuits, Adaptive self tuning filter, Adaptive line enhancer, Adaptive filters for classification and data mining.

**Suggested references** (not limited to)-