• Title of project:
  – Special Manpower Development Project in VLSI Design & Related Software, SMDP-VLSI Phase-2 (Dept. of ECE, MNIT Jaipur)

• Amount sanctioned:
  – Appx. 12 Lakhs/yr; 78 Lakhs total

• Date of award, period: Dec. 2005, 2006-2013

• Funding agency:
  – Ministry of Comm. & IT, Govt. of INDIA (MoCIT)

• Partner institute if any: None

• Names of PI, Co-PIs:
  – PI/Co-PI: Dr. Vineet Sahula, Dr. D. Boolchandani
  – Members: Dr. L. Bhargava, Dr. C. Periasamy
Objective(s): Manpower training

Key deliverables: Designs, Chips, trained manpower (UG/PG)

Major equipment purchased:
- Embedded SW; Logic Analyzer (in process- TEQIP); FPGA/SoC boards
- Xilinx boards & others provided as grant-in-aid as Synopsys, Cadence CAD SW (MoCIT, Govt. of INDIA)

Importance to society/country (2-3 bullets)
- IT Hardware, trained manpower
- Design/product possibility of prototyping electronic hardware
- Emerging as research/development centre in a specific area- Analog Synthesis; System level design/modeling; Low energy electronic systems' prototyping

Major innovation, if any
- Proposed Analog macromodels
- Proposed SoC communication modeling approach
- A chip designed at MNIT Jaipur & fabricated at IMEC Belgium; tested in house at MNIT Jaipur

Patent filed, if any

Photograph of set up/product developed

Snapshot of key analysis (for theoretical projects)
- Proposed Analog macromodels, variability aware accurate models for analog synthesis
- Proposed SoC communication modeling approach, with analytical solution to solve Markov/GSMP models

Main result (s), outcome
- Trained manpower- 05 PhDs; 200+ MTechs; 50 BTechs
- Design/fabricated Hamming CODEC chip

Publications from project
- 20+ Journal and 50+ refereed conference papers
Special Manpower Development Project in VLSI Design & Related Software,
SMDP-VLSI Phase-2

PI/Co-PI: Dr. Vineet Sahula, Dr. D. Boolchandani,
Members: Dr. L. Bhargava, Dr. C. Periasamy
Dept. of ECE, MNIT Jaipur

Funded by: Ministry of Comm. & IT, Govt. of INDIA (MoCIT)
2006-2013
Equipment/Software acquired in Grant-in-aid from MoCIT
(centrally purchased by CEERI, Pilani for IITs/NITs)

• Servers/workstations-
  – high end servers/workstations provided in grant-in-aid by MoCIT
  – 3 servers+ 9 workstations

• Industry standard CAD tools-suites
  – Synopsys, Cadence, Xilinx, Magma, Mentor Graphics,
Equipment/Software purchased/acquired by MNIT Jaipur

- 20 desktops, WIPRO provided by institute (MNITJ)
- Analog/RF design suite from AGILENT under TEQIP
- Embedded design Software
  - Granted by ARM company, Bangalore
  - Granted by Texas Instruments, Bangalore
- Xilinx boards- Vertex-7 and Z-7000 Purchased under TEQIP
- ARM based CORTEX-M boards purchased under TEQIP as well as in grant-in-aid from ARM Inc.
- Texas Microcontroller boards as grant-in-aid from Texas Instruments, Bangalore
Journal Papers Published

• More than 20 in refereed/indexed journals
Journal Papers Published

Indexed & reputed (IEEE, IET, Springer, SPIE etc.)


Conference Papers Published with support of SMDP-VLSI Lab

• More than 60 in refereed conferences
• More than 30 in other conferences/workshops
Refereed Conference Papers in 2013


Refereed Conference Papers 2010-2012


19. D. Boolchandani et al., Chaotic Neural Dynamics as evinced from scalp electroencephalography (EEG) 13th Congress of the European Federation of Neurological Societies (EFNS) ITALY European Journal of Neurology, / 2009

PhD Theses Completed/Continuing

• 4 Theses completed
• 10 are continuing
## PhD Theses Titles

**Dr. Vineet Sahula as Supervisor**

<table>
<thead>
<tr>
<th>Name of the candidate</th>
<th>Title of the thesis</th>
<th>Year completed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ulhas Deshmukh</td>
<td>On Performance Evaluation of SoC Communication Architectures</td>
<td>2010</td>
</tr>
<tr>
<td>D. Boolchandani</td>
<td>On Macro Modeling of Analog Circuits Using Support-Vector-Machines (SVMs) With Efficient Kernels</td>
<td>2011</td>
</tr>
<tr>
<td>Mahanth Prasad</td>
<td>Design, Process Development and Characterization of ZnO-Based MEMS Acoustic Sensor (jt supervisor- Dr. V. K. Khanna)</td>
<td>2013</td>
</tr>
<tr>
<td>Jankiballabh Sharma</td>
<td>Novel approaches for watermarking images &amp; application to image fusion: Use of self-fractional Fourier transforms</td>
<td>2013</td>
</tr>
<tr>
<td>Rajesh A. Patil</td>
<td>Algorithms for Machine Vision and Their Hardware/software Implementation</td>
<td>Continuing</td>
</tr>
<tr>
<td>Renu Kumawat</td>
<td>Nano-Scale Reliable Memory Architectures</td>
<td>Continuing</td>
</tr>
<tr>
<td>Lokesh Garg</td>
<td>Variability Aware System Level Design</td>
<td>Continuing</td>
</tr>
<tr>
<td>Lintu Rajan</td>
<td>Algorithms &amp; Architectures for Cognitive Computing</td>
<td>Continuing</td>
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</tbody>
</table>
## PhD Theses Titles
### Dr. D. Boolchandani as Supervisor

<table>
<thead>
<tr>
<th>Name of the candidate</th>
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<tbody>
<tr>
<td>Seema Yardi</td>
<td>Lab on Chip: Detection of Pathogen From Body Fluid/water/food Using Optical Sensing</td>
<td>Continuing</td>
</tr>
<tr>
<td>Tarun Varma</td>
<td>Fabrication and Characterization of Zinc Oxide Thin Film for Opto Electronic Device Applications.</td>
<td>Continuing</td>
</tr>
<tr>
<td>Vimal Agrawal</td>
<td>Photonic Integrated Circuits</td>
<td>Continuing</td>
</tr>
<tr>
<td>Sapna Khandelwal</td>
<td>Reliability and Process Aware SVM Based Macro Models for Analog Circuits</td>
<td>Continuing</td>
</tr>
<tr>
<td>Yashwant Singh</td>
<td>Design of Low Leakage SRAM Circuits With Improved Yield and Reliability</td>
<td>Continuing</td>
</tr>
</tbody>
</table>
### PhD Theses Titles - Dr. C. Periasamy as Supervisor

<table>
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<tr>
<th>Name of the candidate</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Shahikant</td>
<td>Design, Fabrication and Characterization of Nanostructured ZnO Thin Film Based Electronic Devices.</td>
<td>Continuing</td>
</tr>
</tbody>
</table>
MTech Theses Completed/Continuing

• About more than 200 theses completed since 2005 MTech VLSI Design programme started

• Currently, 30 theses students are continuing as full time; appx. 5 as part time
# Select MTech Theses Titles - Dr. V. Sahula as Supervisor

<table>
<thead>
<tr>
<th>Name of the candidate</th>
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<th>Year completed</th>
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</thead>
<tbody>
<tr>
<td>Amit Kumar</td>
<td>Secondary effects in nanoscale devices</td>
<td>2012</td>
</tr>
<tr>
<td>Anuj Solanki</td>
<td>Variability aware Memory yield enhancement</td>
<td>2012</td>
</tr>
<tr>
<td>Mahesh Soni</td>
<td>Memory synthesis using nanodevices</td>
<td>2012</td>
</tr>
<tr>
<td>Rajesh Sahu</td>
<td>Analog synthesis into nanometer</td>
<td>2012</td>
</tr>
<tr>
<td>B. Gopikrishna</td>
<td>Design &amp; Verification of Mobile High definition Link Interface</td>
<td>2013</td>
</tr>
<tr>
<td>A. Mallikarjuna Reddy</td>
<td>IMPLEMENTATION OF eMMC 5.0 FEATURES FOR THE MOBILE STORAGE IP</td>
<td>2013</td>
</tr>
<tr>
<td>Ramesh Kumar</td>
<td>Design an Ultra Low Power Low Phase Noise Lc Voltage Controlled Oscillator</td>
<td>2013</td>
</tr>
<tr>
<td>K. Swaraj Gowtham</td>
<td>Efficient utilization of power in a Phase-Locked Loop Design</td>
<td>2013</td>
</tr>
<tr>
<td>Saima Cherukat</td>
<td>Modeling and Design in Ultra Deep SubMicron Technology- (a) Variation robust ultra low power Novel SRAM Cell (b) Proposing Models and order reduction of models for SoC interconnects</td>
<td>2013</td>
</tr>
</tbody>
</table>
Select MTech Theses Titles-
Dr. D. Boolchandani as Supervisor

<table>
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<th>Name of the candidate</th>
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<tbody>
<tr>
<td>Shivani Yadav</td>
<td>Modeling and Simulation of CMOS Logic Circuits Using ANN &amp; ANFIS</td>
<td>2012</td>
</tr>
</tbody>
</table>
Select MTech Theses Titles - Dr. L. Bhargava as Supervisor

<table>
<thead>
<tr>
<th>Name of the candidate</th>
<th>Title of the thesis</th>
<th>Year completed</th>
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<tbody>
<tr>
<td>Vidhi Agrawal</td>
<td>Hardware Implementation of binary LDPC Encoder</td>
<td>2012</td>
</tr>
<tr>
<td>Ashish Sharma</td>
<td>Hardware Implementation of binary LDPC Encoder</td>
<td>2012</td>
</tr>
<tr>
<td>Noor-Ul-Mustafa</td>
<td>Hardware Implementation and Performance Analysis of Non-Binary LDPC Decoder</td>
<td>2012</td>
</tr>
<tr>
<td>Name of the candidate</td>
<td>Title of the thesis</td>
<td>Year completed</td>
</tr>
<tr>
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</tr>
<tr>
<td>Mr. Nannepamula Suresh</td>
<td>Ground Bounce Noise aware Forward Body Biased MTCMOS Circuit Techniques for Combinational Circuits</td>
<td>2013</td>
</tr>
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</table>